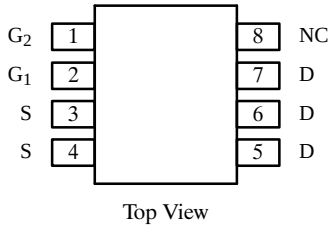
Dual Gate, N-Channel Enhancement-Mode MOSFET

Product Summary

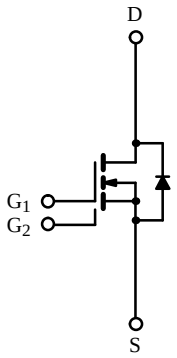
	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
Gate 1	30	0.022 @ V_{GS} = 10 V	± 7.7
		0.03 @ V_{GS} = 4.5 V	± 6.4
Gate 2		0.25 @ V_{GS} = 10 V	± 2.0
		0.40 @ V_{GS} = 4.5 V	± 1.5

TrenchFET™ Power MOSFETs

SO-8



Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Gate 1	Gate 2	Unit
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	± 7.7	± 6.4	A
	T_A = 70°C		± 4.4	± 6.0	
Pulsed Drain Current		I_{DM}	± 40	± 4.0	
Continuous Source Current (Diode Conduction)[a]		I_S	2		
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.3		W
	T_A = 70°C		1.0		
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	Gate 1 or Gate 2	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	55	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70657.

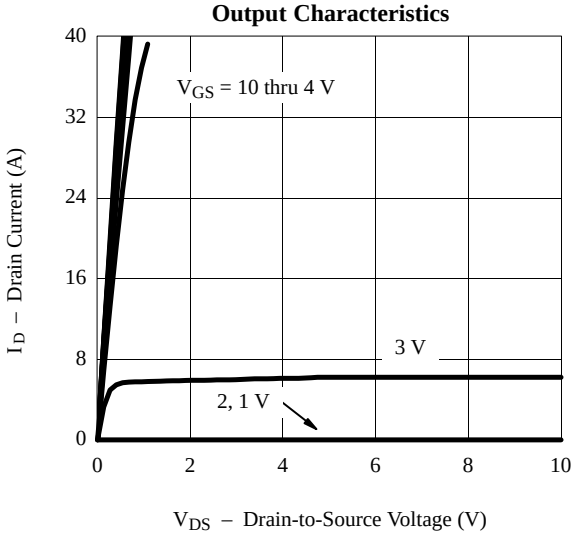
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		1			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V				1	µA
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55°C				5	
On-State Drain Current[a]	$I_{D(on)}$	(G_1 = G_2) V_{DS} = 5 V, V_{GS} = 10 V		40			A
Drain-Source On-State Resistance[a]	$r_{DS1(on)}$	(G_1 = G_2) V_{GS} = 10 V, I_D = 7.7 A			0.017	0.022	Ω
		(G_1 = G_2) V_{GS} = 4.5 V, I_D = 6.4 A			0.021	0.03	
	$r_{DS2(on)}$	V_{G1S} = 0 V, V_{G2S} = 10 V, I_D = 2.0 A			0.20	0.25	
		V_{G1S} = 0 V, V_{G2S} = 4.5 V, I_D = 0.3 A			0.30	0.40	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 7.7 A			21		S
Diode Forward Voltage[a]	V_{SD}	I_S = 2 A, V_{GS} = 0 V			0.72	1.1	V
Dynamic[b]							
Total Gate Charge	Q_g	Gate 1 V_{DS} = 15 V, $V_{GS(1,2)}$ = 10 V, I_D = 7.7 A	Gate 1		34	60	nC
			Gate 2		2.2	5	
Gate-Source Charge	Q_{gs}		Gate 1		6.5		
		Gate 2 V_{DS} = 15 V, $V_{GS(1)}$ = 0 V, $V_{GS(2)}$ = 10 V, I_D = 2.0 A	Gate 2		0.5		
Gate-Drain Charge	Q_{gd}		Gate 1		5.2		
			Gate 2		0.28		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 15 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω			12	15	ns
Rise Time	t_r				9	20	
Turn-Off Delay Time	$t_{d(off)}$				55	80	
Fall Time	t_f				15	30	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 2 A, di/dt = 100 A/µs			40	60	

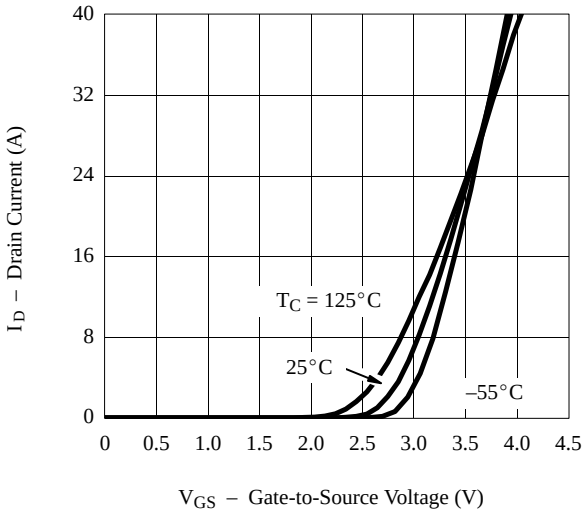
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Typical Characteristics ($V_{G1} = V_{G2}$, 25°C Unless Noted)

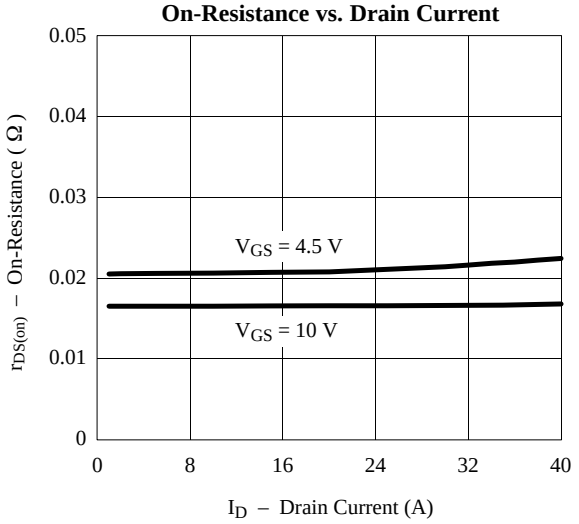
Output Characteristics



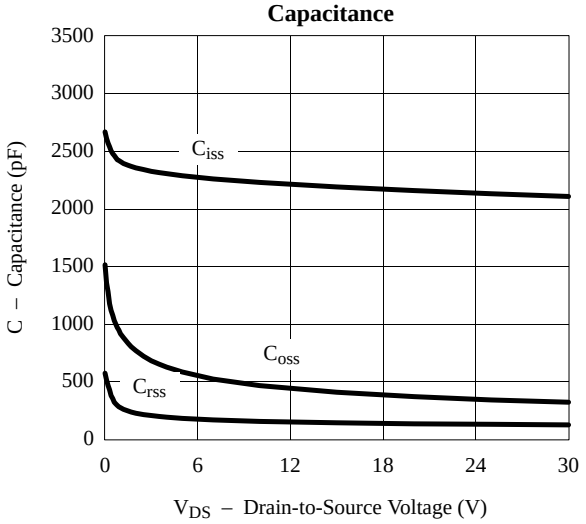
Transfer Characteristics



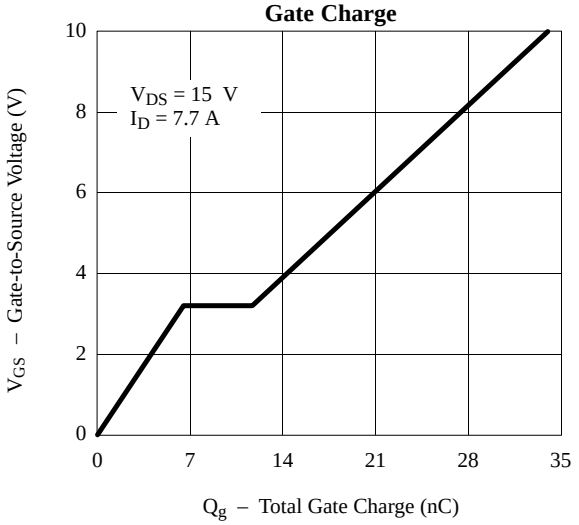
On-Resistance vs. Drain Current



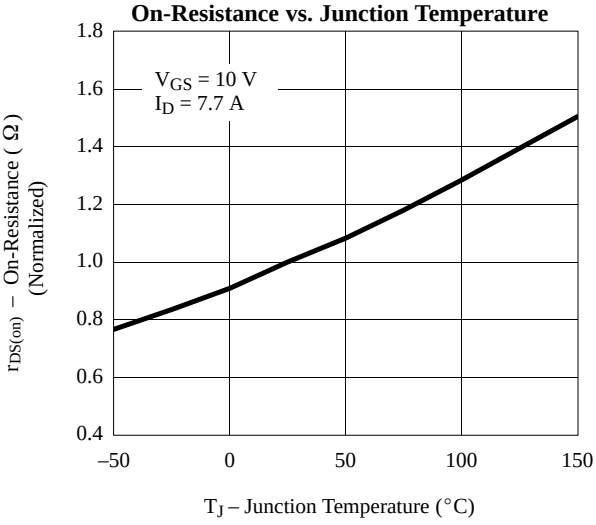
Capacitance



Gate Charge

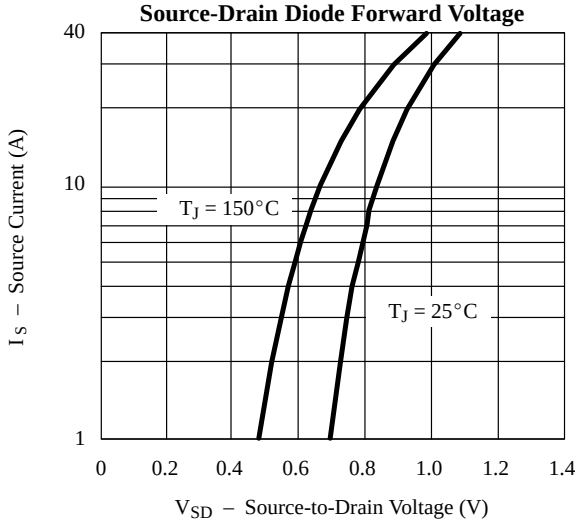


On-Resistance vs. Junction Temperature

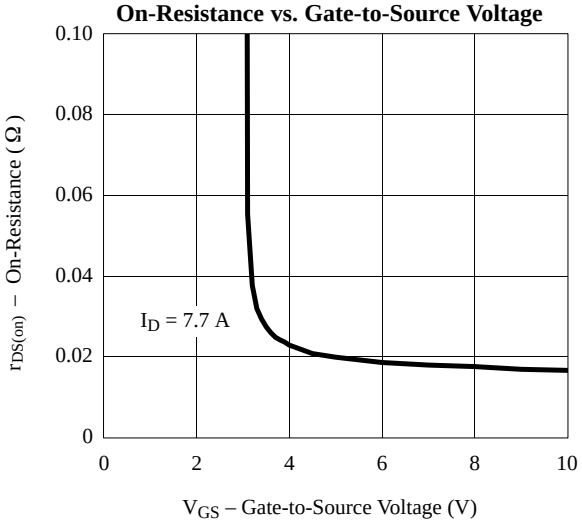


Typical Characteristics ($V_{G1} = V_{G2}$, 25°C Unless Otherwise Noted)

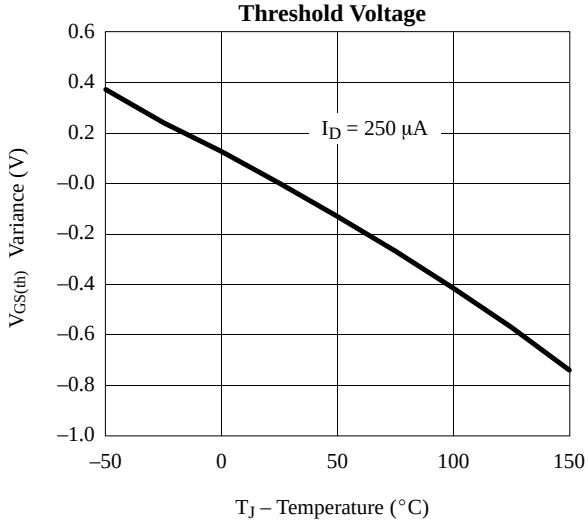
Source-Drain Diode Forward Voltage



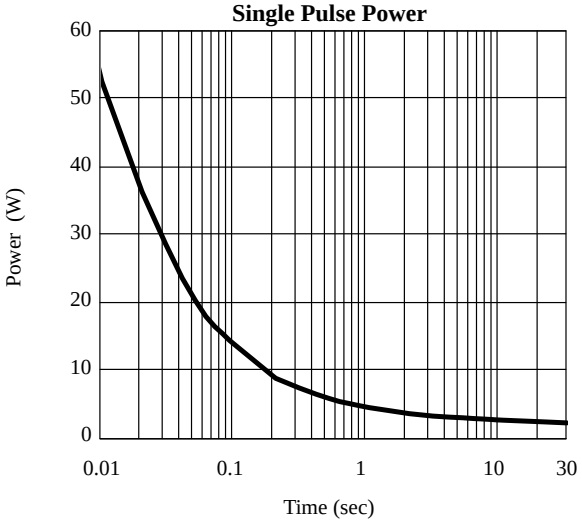
On-Resistance vs. Gate-to-Source Voltage



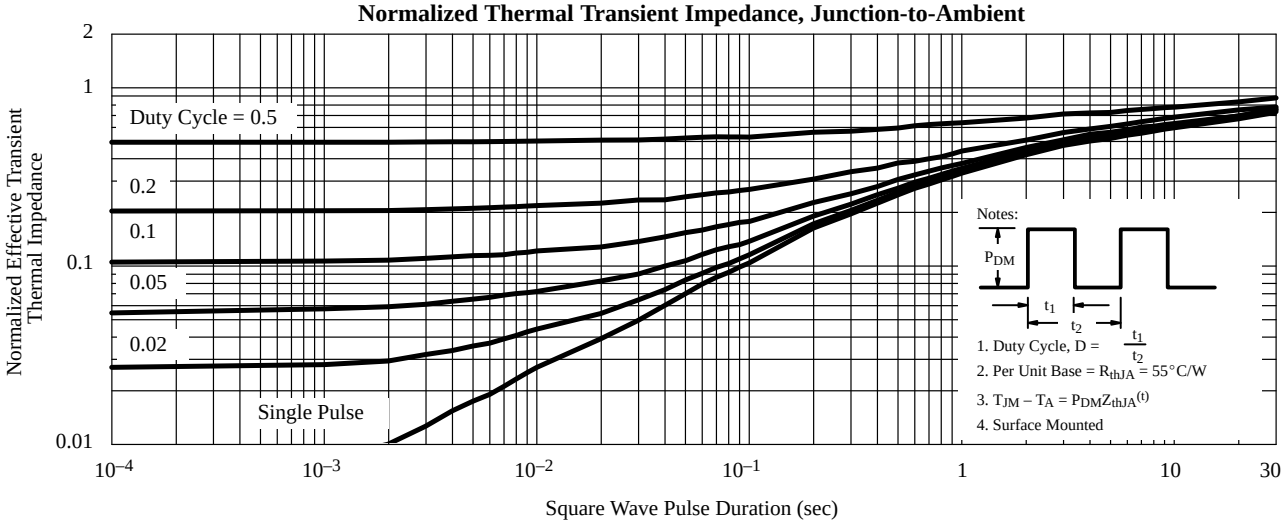
Threshold Voltage



Single Pulse Power

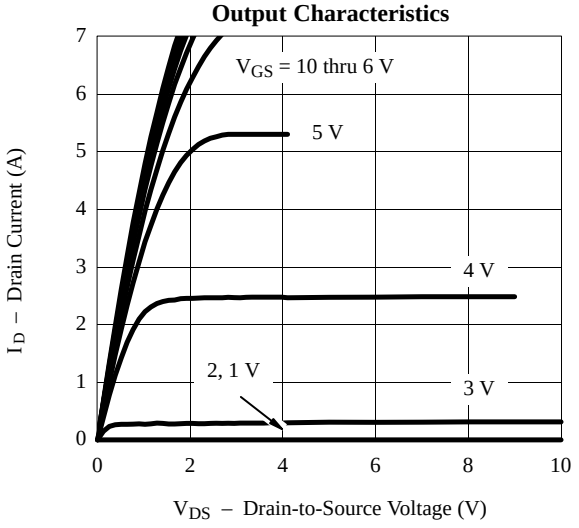


Normalized Thermal Transient Impedance, Junction-to-Ambient

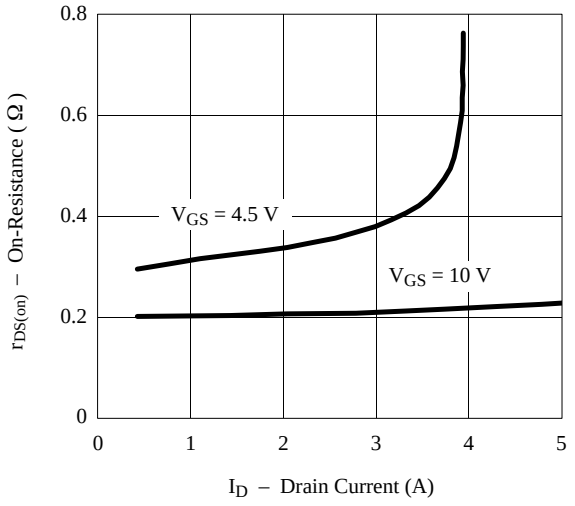


Typical Characteristics (V_{G1} = 0 V, 25°C Unless Noted)

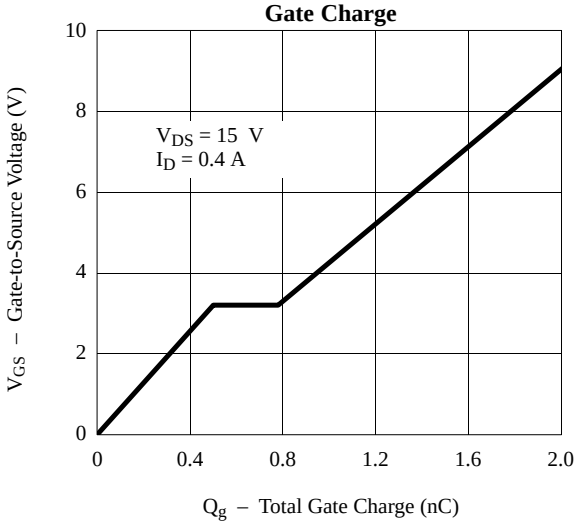
Output Characteristics



On-Resistance vs. Drain Current



Gate Charge



On-Resistance vs. Gate-to-Source Voltage